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10/724,817	11/24/2003	Lars Risbo	TI-34411	2748
23494 7590 02/06/2009 TEXAS INSTRUMENTS INCORPORATED P O BOX 655474, M/S 3999 DALLAS, TX 75265				
EXAMINER				
GHULAMALL QUTBUDDIN				
ART UNIT		PAPER NUMBER		
2611				
NOTIFICATION DATE		DELIVERY MODE		
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

uspto@ti.com

Office Action Summary

Application No.

10/724,817

Applicant(s)

RISBO ET AL.

Examiner

Qutbuddin Ghulamali

Art Unit

2611

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 10 November 2008.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-26 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☒ Claim(s) 9-12 is/are allowed.
- 6) ☒ Claim(s) 1-8, 13-26 is/are rejected.
- 7) ☒ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO-8508)
Paper No(s)/Mail Date _____

- 4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date _____
- 5) ☐ Notice of Informal Patent Application
- 6) ☐ Other: _____

DETAILED ACTION

1. This office action is in response to amendment filed 11/10/2008.

Response to Arguments

2. Applicant's remarks, page 11-12 with respect to Ihs does not qualify as a prior art for the rejection of claims 1-8, 13-22, 25-26 have been fully considered and is persuasive. However, remarks are moot in view of the new ground(s) of rejection. The rejection based on the new art follows.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

4. Claims 1-4, 13-16, 18-26 are rejected under 35 U.S.C. 102 (e) as being anticipated by Sheen (USP 6,404,369).

Regarding claims 1, 2, Sheen discloses a compensation system programmed to mitigate errors, associated with a digital-to-analog converter (DAC), the compensation system comprising:

a digital error model (fig. 2, DAC error model 222) programmed to provide an emulated error signal as a function of an input signal that is provided to the DAC (col. 3, lines 15-25; col. 4, lines 35-44), the input signal being quantized in a predetermined number of one or more levels, the digital error model parameterized by an error coefficient vector that includes a plurality of error coefficients (col. 4, lines 60-67), at least a portion of the plurality of error coefficients are adaptively adjusted based at least in part on the input signal of to the system DAC to emulate error characteristics associated with the DAC (col. 4, lines 35-67), Sheen further discloses a memory that stores a digital error model (col. 4, lines 60-67; col. 5, lines 1-11).

Regarding claim 3, Sheen discloses the signal of the DAC is an output signal (fig. 4, element 218, 222).

Regarding claim 4, Sheen discloses a compensation system programmed and/or configured to mitigate errors in conversion comprising:

a digital error model (fig. 2, DAC error model 222) configured to provide an emulated error signal as a function of an function of an input signal that is quantized in a predetermined number of one or more levels, the digital error model having parameters adaptively adjusted based on a signal of the conversion system to emulate error characteristics associated with at least a portion of the conversion system (col. 3, lines 15-25; col. 4, lines 35-44), and the parameters of the digital error model being adapted

to converge to respective values that substantially minimize errors in an output signal of the conversion system over a plurality of iterations (col. 5, lines 43-64).

Regarding claim 13, Sheen discloses all limitations of the claim above. Sheen further discloses a DAC (fig. 2, DAC 216) coupled to receive the input signal that is quantized (quantizer 214) in the predetermined number of levels and to convert the input signal to a corresponding analog output signal, the error characteristics being error.

Regarding claim 14, Sheen discloses a noise and error shaping filter (filter 212) that receives a digital signal and provides a filtered digital signal for conversion into the corresponding analog signal;
a quantizer (214) that provides a quantized signal to DAC (216, 222) based on filtered digital signal, and provide emulated error signal shaping module as a function of quantized signal (col. 3, lines 15-20).

Regarding claim 15, Sheen discloses a compensation system programmed and/or configured to mitigate errors in conversion comprising:
a digital error model (DAC 222) configured to provide an emulated error signal as a function of an function of an input signal that is quantized (quantizer 214) in a predetermined number of one or more levels, the digital error model having parameters adaptively adjusted (adjust to match expected values) based on a signal of the conversion system to emulate error characteristics associated with at least a portion of the conversion system (col. 4, lines 35-44); a DAC (216, 222) coupled to receive the input signal that is quantized (214) in the predetermined number of levels and to convert

the input signal to a corresponding analog output signal, the error characteristics being error characteristics associated with the DAC (col. 3, lines 20-24; col. 4, lines 60-67); and a calibration system (calibration routine) that calibrates the parameters of the digital error model in a calibration mode based on content of an output signal of the conversion system in response to a calibration signal provided to the conversion system (col. 5, lines 1-12).

Regarding claim 16, Sheen discloses a compensation system programmed and/or configured to mitigate errors in conversion comprising:
a digital error model (DAC 222) configured to provide an emulated error signal as a function of an input signal that is quantized (quantizer 214) in a predetermined number of one or more levels, the digital error model having parameters adaptively adjusted (adjust to match expected values) based on a signal of the conversion system to emulate error characteristics associated with at least a portion of the conversion system (col. 4, lines 35-44); a DAC (216, 222) coupled to receive the input signal that is quantized (214) in the predetermined number of levels and to convert the input signal to a corresponding analog output signal, the error characteristics being error characteristics associated with the DAC (col. 3, lines 20-24; col. 4, lines 60-67); a calibration system (calibration routine) that calibrates the parameters of the digital error model in a calibration mode based on content of an output signal of the conversion system in response to a calibration signal provided to the conversion system (col. 5, lines 1-12); an analog filter to remove out of band frequencies and quantize signal from corresponding analog output filtered signal (fig. 2, element 212).

5. Claim 17 are rejected under 35 U.S.C. 103 (a) as being unpatentable over Sheen (USP 6,404,369) in view of Sooch et al (USP 5,061,925).

Regarding claim 17, Sheen discloses a compensation system programmed and/or configured to mitigate errors in conversion comprising:

a digital error model (DAC 222) configured to provide an emulated error signal as a function of an function of an input signal that is quantized in a predetermined number of one or more levels, the digital error model having parameters adaptively adjusted based on a signal of the conversion system to emulate error characteristics associated with at least a portion of the conversion system (col. 4, lines 35-44); a DAC (216, 222) coupled to receive the input signal that is quantized (214) in the predetermined number of levels and to convert the input signal to a corresponding analog output signal, the error characteristics being error characteristics associated with the DAC (col. 3, lines 20-24; col. 4, lines 60-67);

a calibration system that calibrates the parameters of the digital error model in a calibration mode based on content of an output signal of the conversion system in response to a calibration signal provided to the conversion system (col. 5, lines 1-12).

Sheen does not disclose at least two capacitors for DAC. However, Sooch discloses a plurality of capacitors (fig. 4, switched capacitor stages 110, 112, 114 and 116) (col. 6, lines 46-68; col. 7, lines 1-18). It would have been obvious to a person of ordinary skill in the art at the time the invention was made to use capacitors as taught by Sooch in

the system of Sheen because it can provide effective mitigation in error with the digital error signals.

Regarding claim 18, Sheen discloses a compensation system programmed and/or configured to mitigate errors in conversion comprising:
a digital error model (DAC 222) configured to provide an emulated error signal as a function of an function of an input signal that is quantized in a predetermined number of one or more levels, the digital error model having parameters adaptively adjusted based on a signal of the conversion system to emulate error characteristics associated with at least a portion of the conversion system (col. 4, lines 35-44); a DAC (216, 222); a noise shaping filter (212) that receives an analog input signal (col. 6, lines 26-33); a DAC (216, 222) coupled to receive the input signal that is quantized (quantizer 214) in the predetermined number of levels and to convert the input signal to a corresponding analog output signal, the error characteristics being error characteristics associated with the DAC (col. 3, lines 20-24; col. 4, lines 60-67);
a calibration system that calibrates the parameters of the digital error model in a calibration mode based on content of an output signal of the conversion system in response to a calibration signal provided to the conversion system (col. 5, lines 1-12).

Regarding claims 19-22, 25, and 26, Sheen discloses digital filter provide filtering output signal of the conversion system to provide residual error signal substantially free of out-band frequencies (col. 3, lines 54-63); a calibration system that calibrates and estimates the parameters of the digital error model in a calibration mode based on

content of an output signal of the conversion system in response to a calibration signal provided to the conversion system (col. 5, lines 1-12).

Regarding claims 23 and 24, Sheen discloses a calibration system that calibrates the parameters of the digital error model in a calibration mode based on content of an output signal of the conversion system in response to a calibration signal provided to the conversion system (col. 5, lines 1-12).

6. Claims 5, 6, 7, 8 are rejected under 35 U.S.C. 103 (a) as being unpatentable over Sheen (USP 6,404,369) in view of Endres et al (US Pub. 2004/0190649).

Regarding claims 5-8, Sheen discloses a compensation system programmed and/or configured to mitigate errors in conversion comprising:
a digital error model (DAC 222) configured to provide an emulated error signal as a function of an function of an input signal that is quantized in a predetermined number of one or more levels, the digital error model having parameters adaptively adjusted based on a signal of the conversion system to emulate error characteristics associated with at least a portion of the conversion system (col. 4, lines 35-44). Sheen does not explicitly disclose a splitter to divide the input signal into a plurality of intermediate signals and a multi input single output (multiplexer) to combine the intermediate signals for providing the emulated error signal. However, Endres discloses a splitter operative to divide the input signal into plural intermediate signals (page 12, section 0179); and a multi-input single output system (multiplexer 910) that employs the parameters of the digital error model to combine the intermediate signals for providing the emulated error signal (page

12, section 0179). It would have been obvious to a person of ordinary skill in the art at the time the invention was made to use a splitter to split the signal and use a multiplexer to multiplex the plurality of intermediate split signals to combine to produce an error signal as taught by Endres in the system of Sheen because it can effectively provide or create an error signal for compensation of the input signal minimize error in the overall output signal.

Allowable Subject Matter

7. Claims 9-12 allowed.

Conclusion

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Qutbuddin Ghulamali whose telephone number is (571)-272-3014. The examiner can normally be reached on Monday-Friday, 7:00AM - 4:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chieh M. Fan can be reached on (571) 272-3042. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

QG.
February 1, 2009.

/Chieh M Fan/
Supervisory Patent Examiner, Art Unit 2611